

Fig. 3
 Prior art

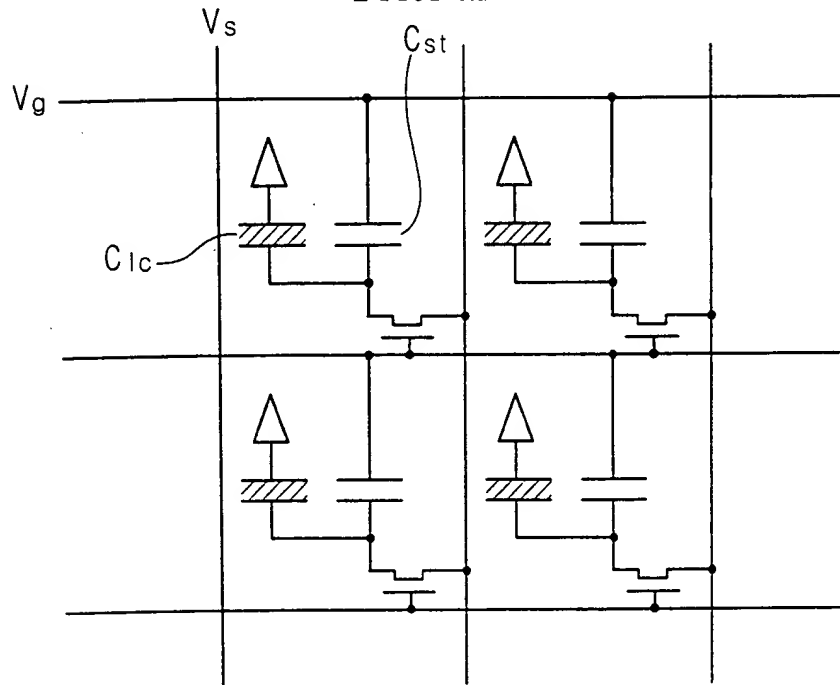


Fig. 4
 Prior art

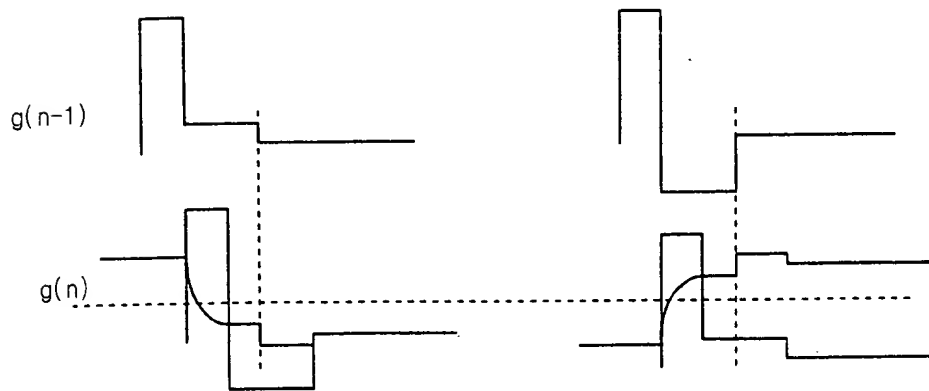
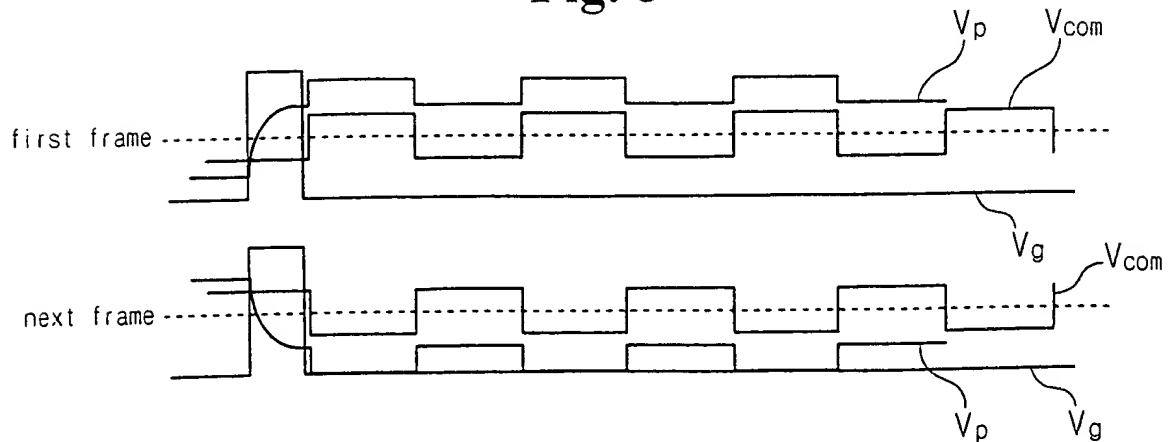


Fig. 5



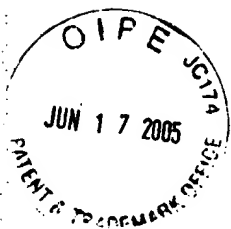


Fig. 6

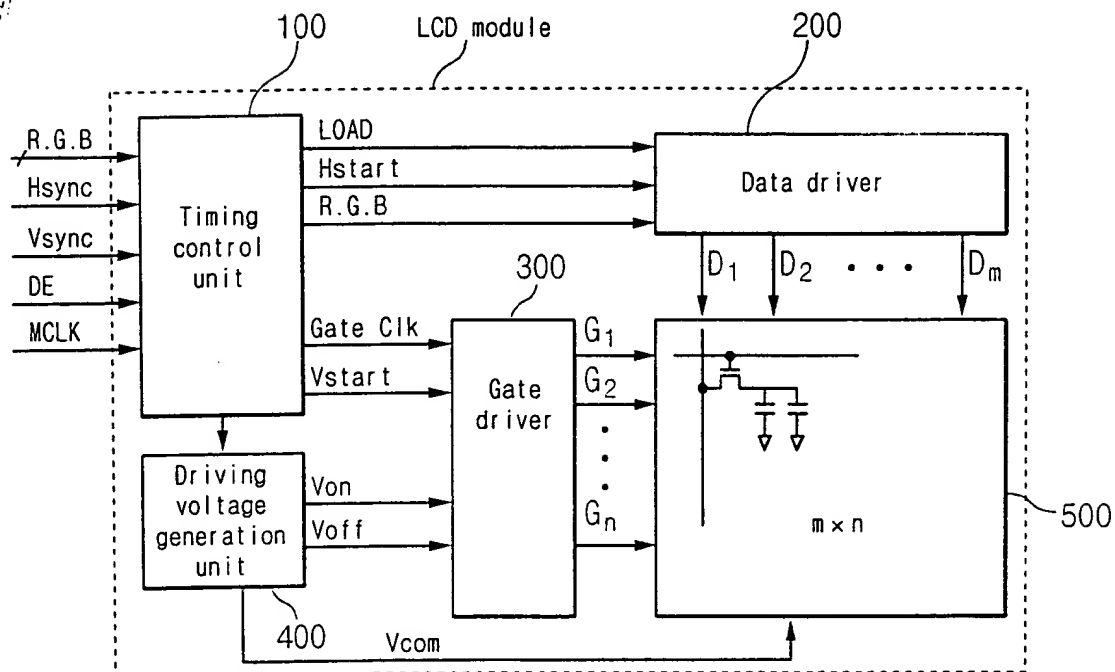


Fig. 7

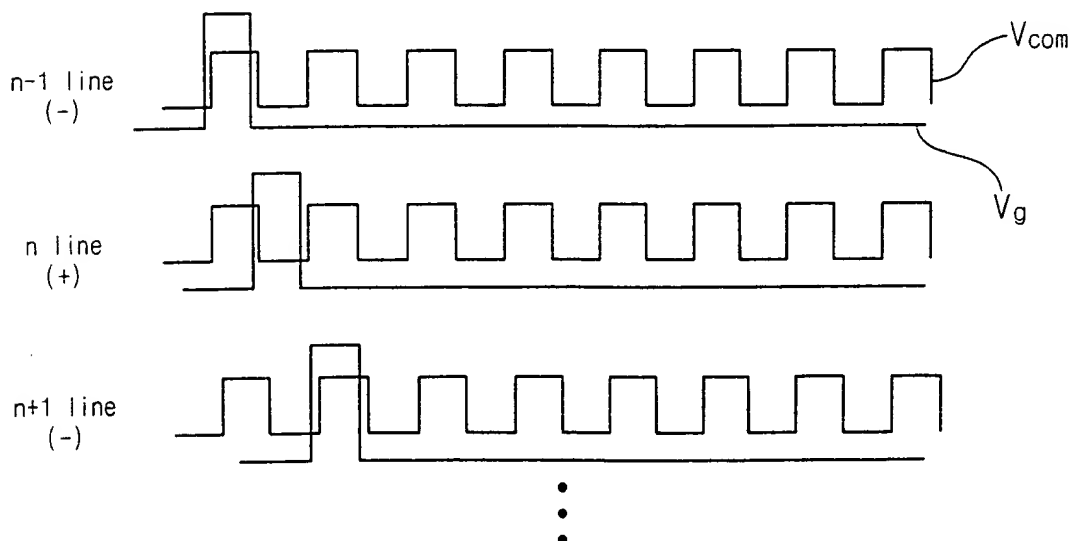




Fig. 8

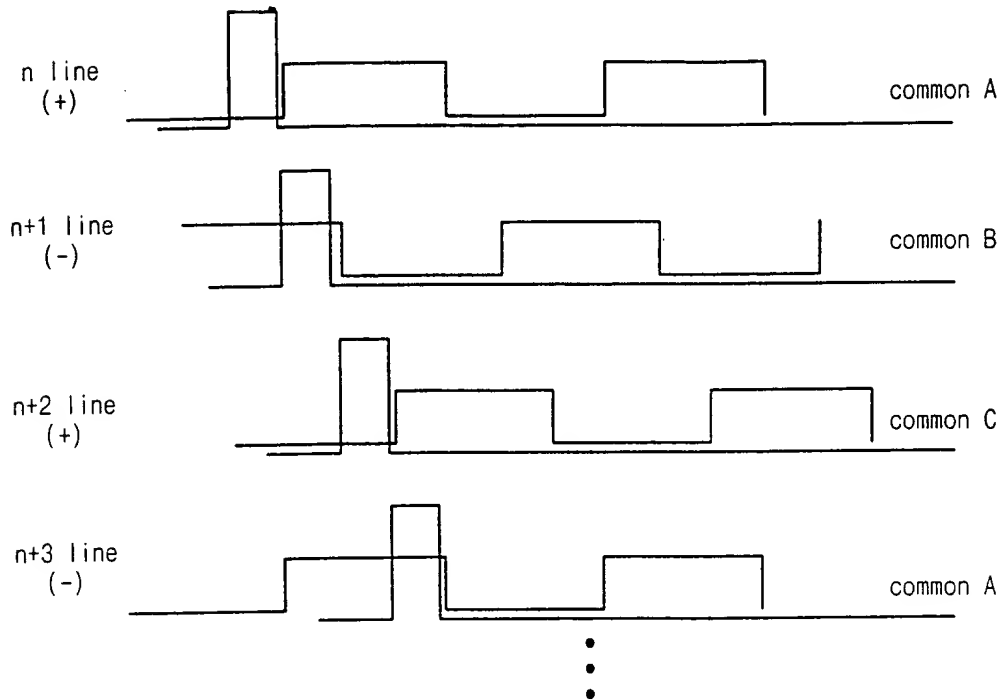


Fig. 9

Prior art

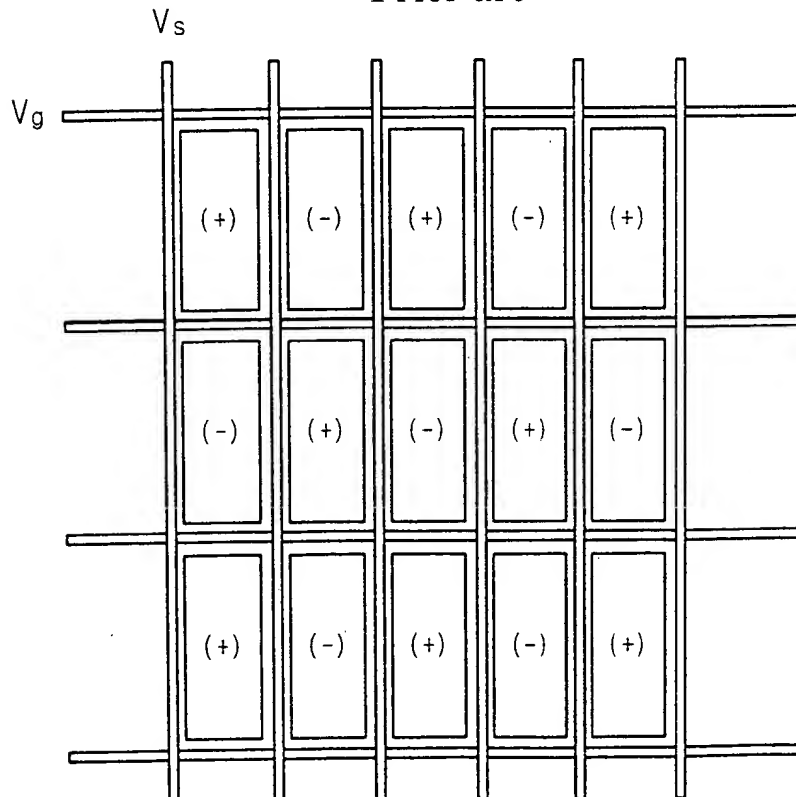




Fig. 10

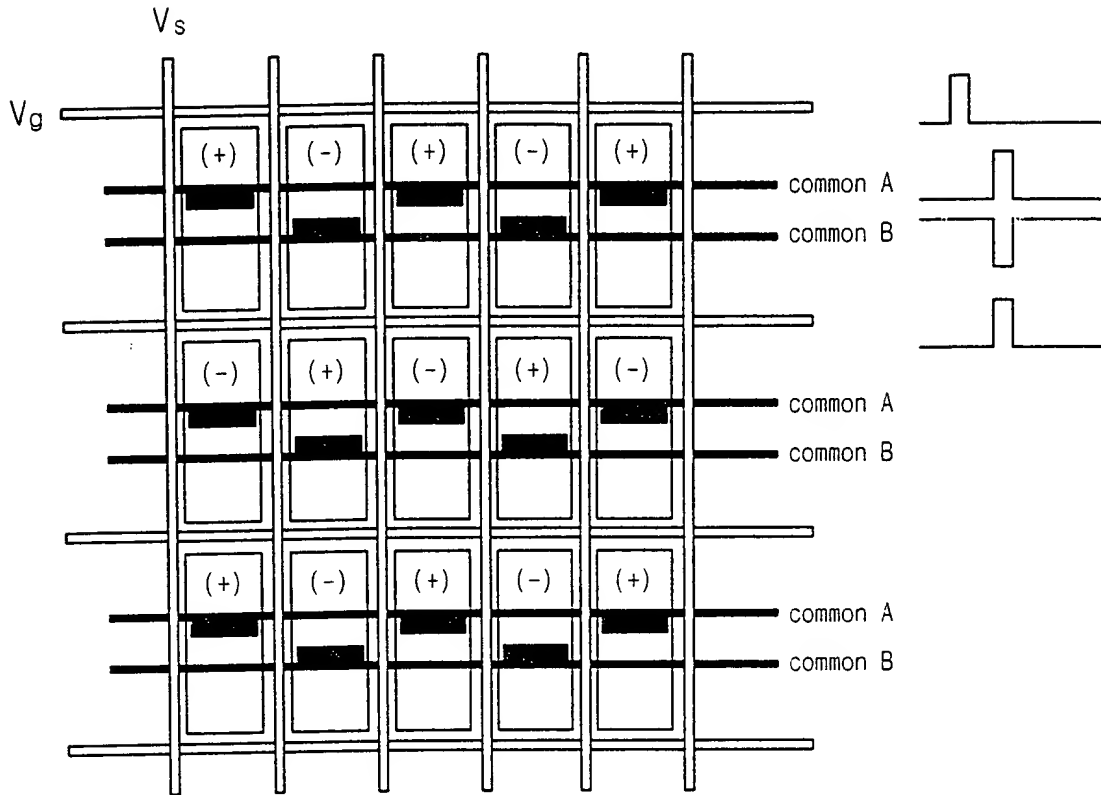


Fig. 11

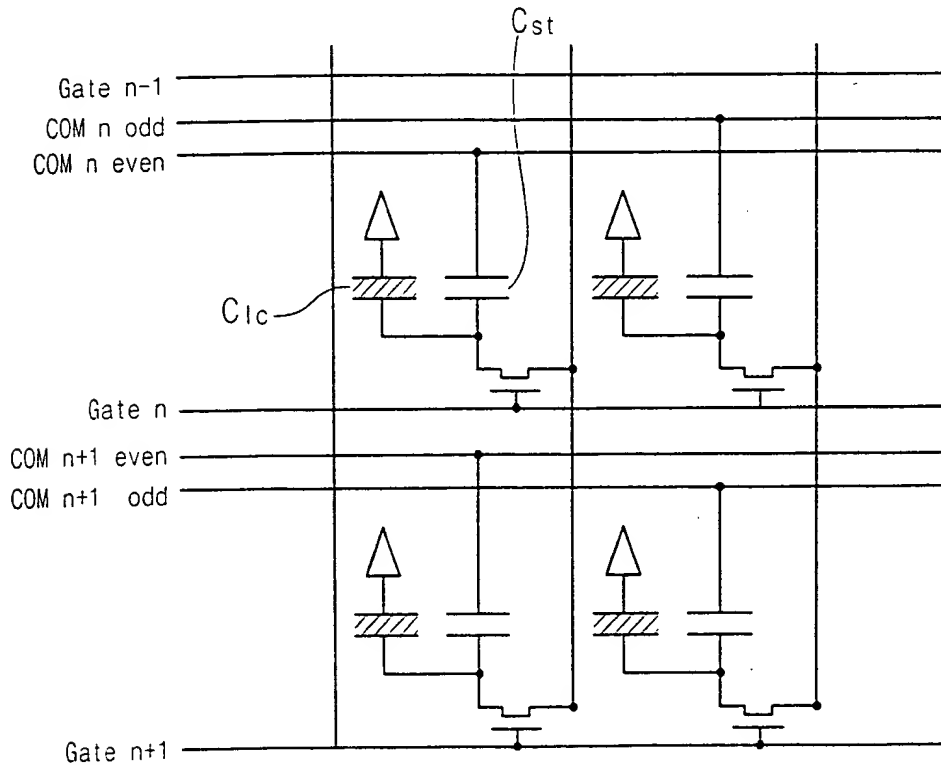




Fig. 12

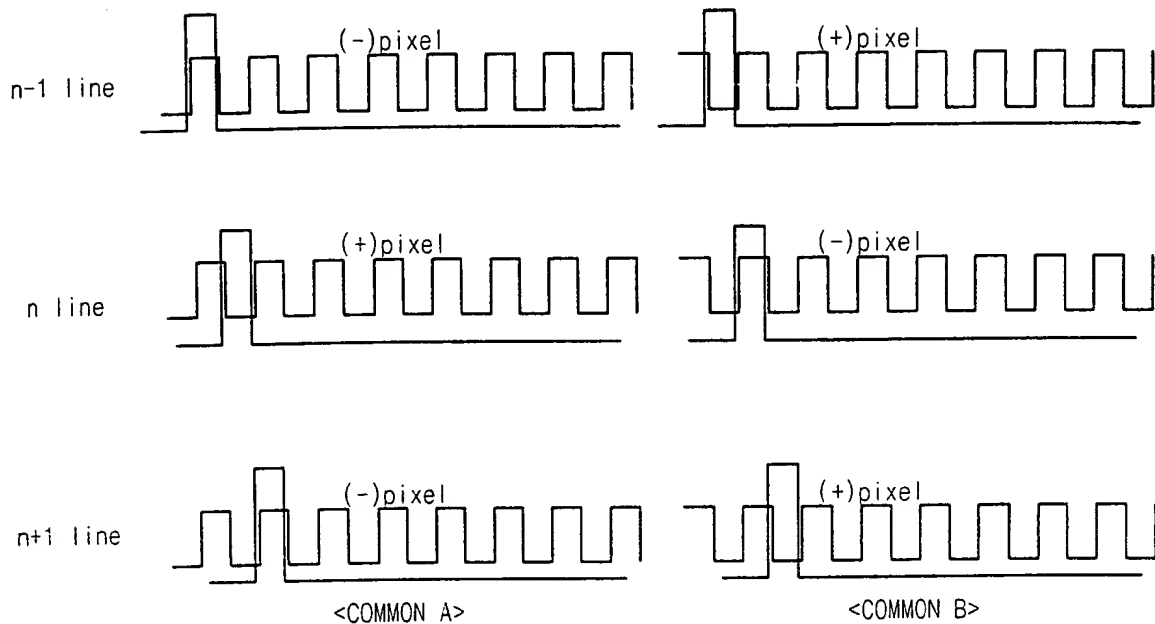


Fig. 13

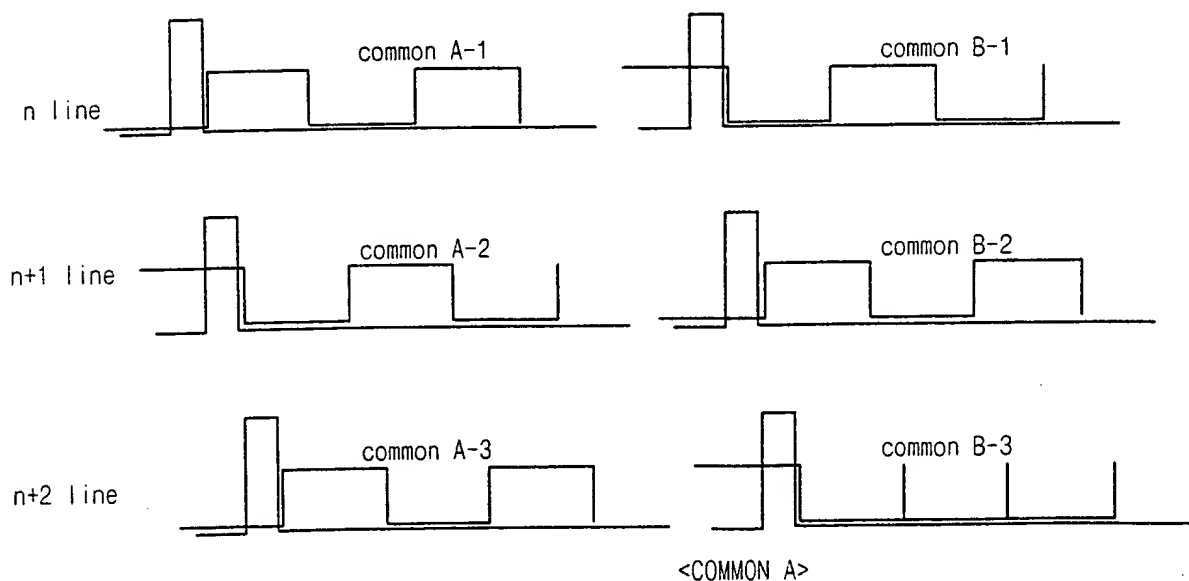




Fig. 14.

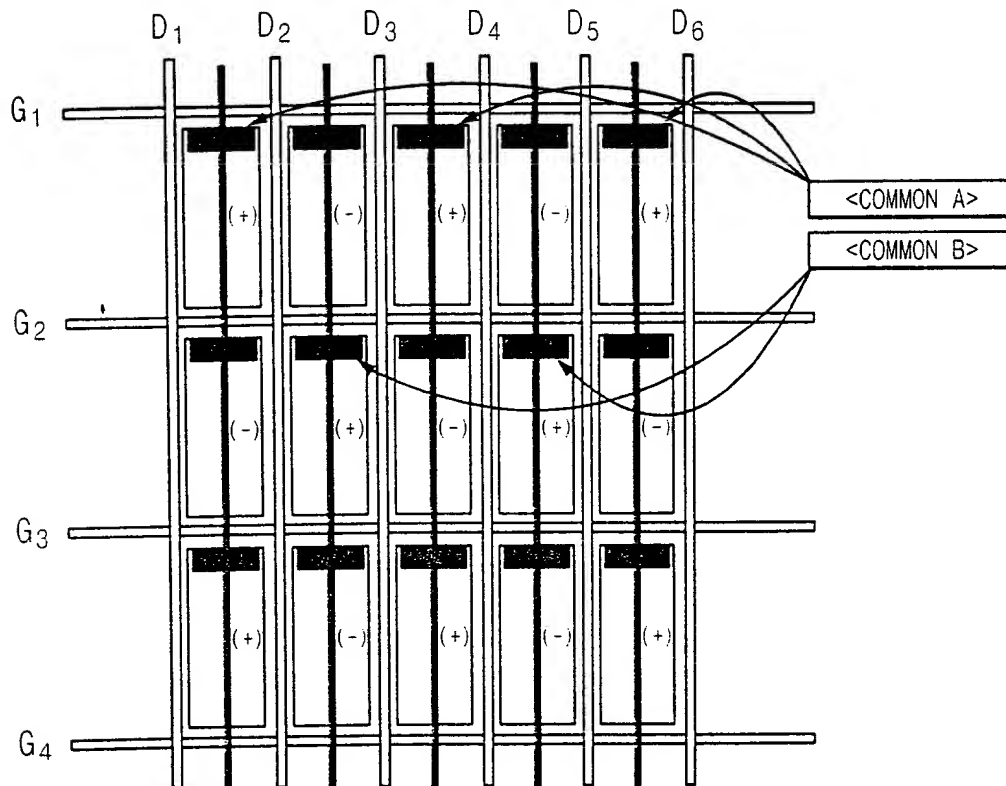




Fig. 15

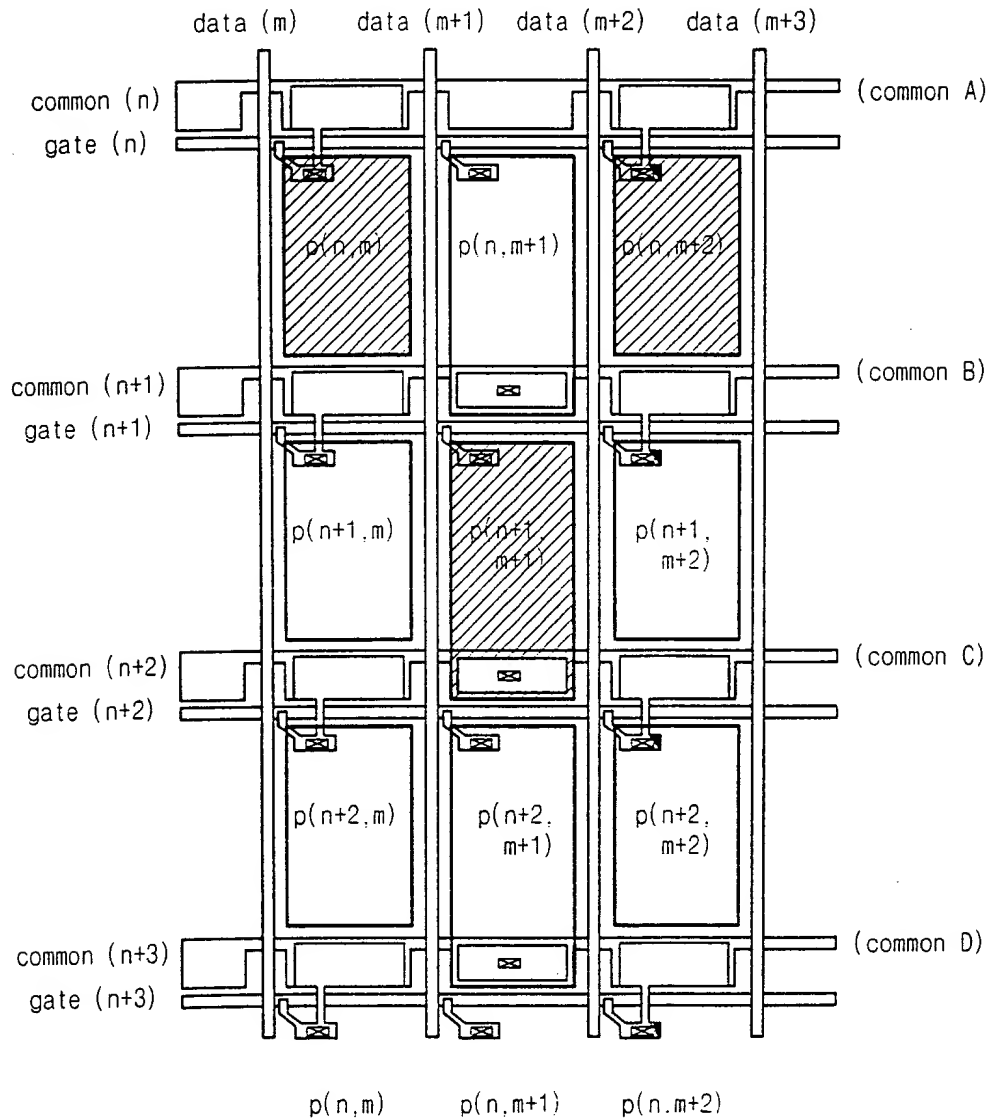
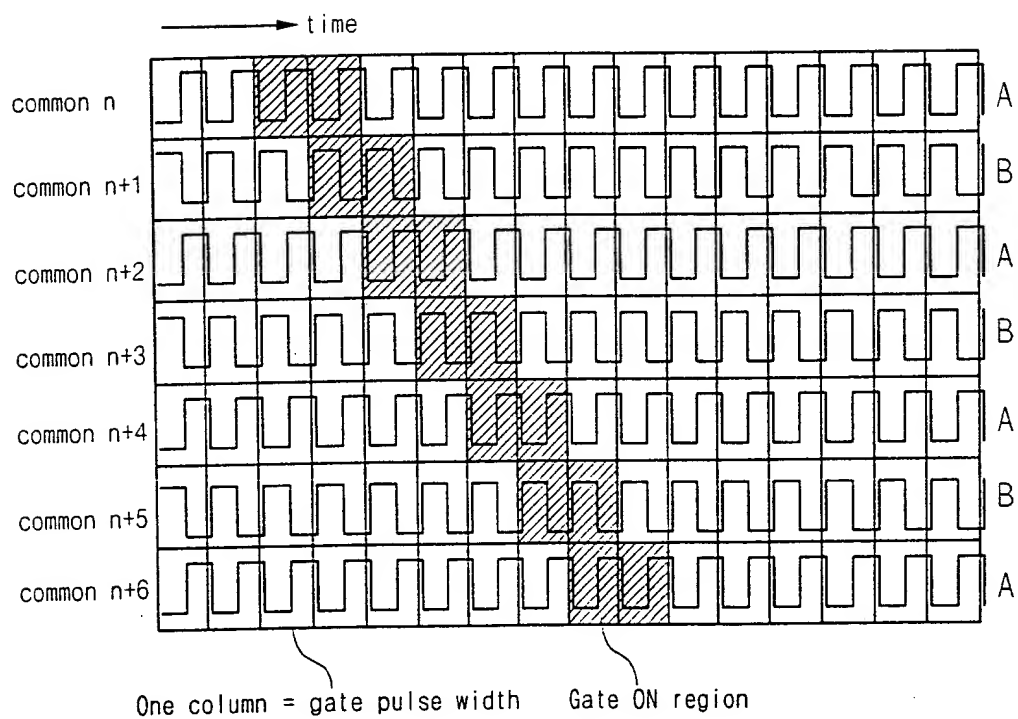




Fig. 16



Timing diagram showing gate pulse widths and ON regions for common n through common n+6. The diagram is a grid with time on the horizontal axis. Each row represents a common signal. The shaded regions indicate the gate pulse width, and the regions where the signal is high indicate the gate ON region. The diagram shows that the gate pulse width is constant for all common signals, and the gate ON region is also constant for all common signals.

The diagram shows four digital signals over time. The signals are labeled 'common n', 'common n+1', 'common n+2', and 'A'. The signals are represented by horizontal lines with vertical steps indicating transitions. Shaded regions are present in the first three signals, indicating specific time intervals. The signal 'A' is shown at the bottom, with a shaded region in the first interval.

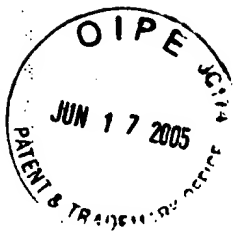


Fig. 19

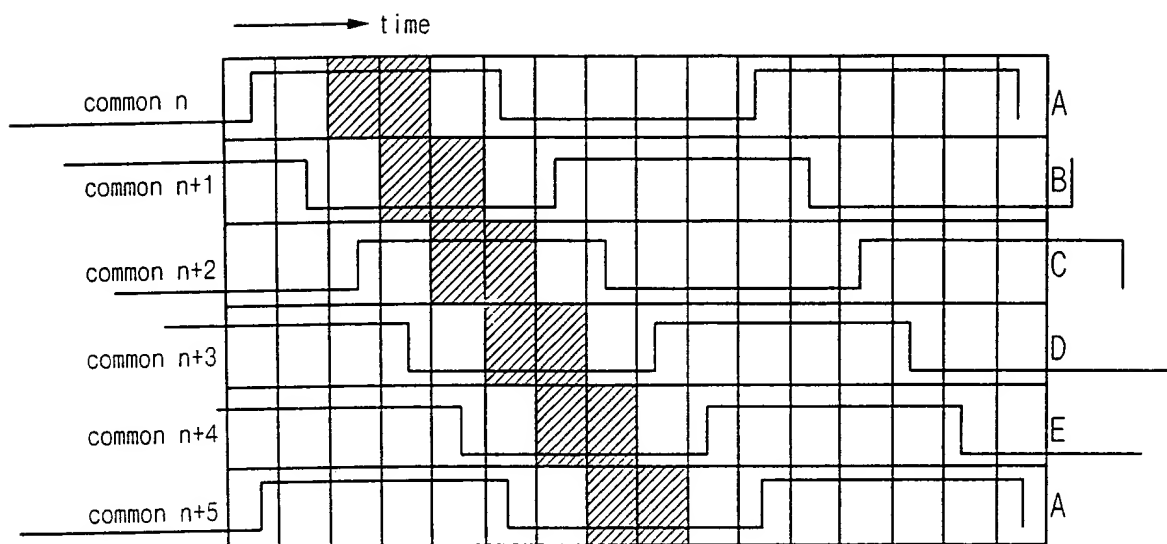


Fig. 20

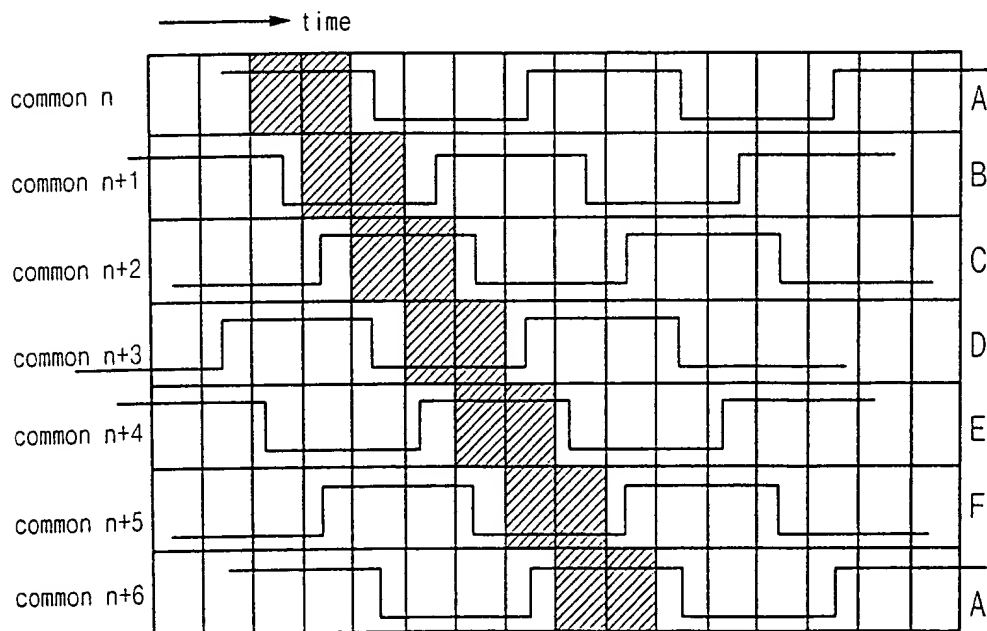




Fig. 21

